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WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a bulk region formed in a semiconductor substrate; and

a semiconductor region formed on one of a buried insulating film in said semiconductor substrate and a cavity region formed in said semiconductor substrate;

said bulk region including:

a memory cell array having a plurality of memory cells arranged in the form of a matrix and including a plurality of memory cells connected to bit lines and word lines;

sense amplifier connected to said bit lines of said memory cell array, said sense amplifier being adapted to sense and amplify the potentials of said bit lines; and

column selection gate for connecting said sense amplifier to first data line;

said semiconductor region including:

word line selection circuit for selecting appropriate ones of said word lines; and

column selection circuit for selecting appropriate ones of said column selection gate.

2. The device according to claim 1, wherein

said bulk region is substantially rectangular shape and said semiconductor region is located along two sides of said bulk region.

3. The device according to claim 1, wherein said semiconductor region contains a switch circuit for switching from defective first data line to spare first data line.

4. A semiconductor device comprising:

a bulk region formed in a semiconductor substrate; and

a semiconductor region formed on one of a buried insulating film in said semiconductor substrate and a cavity formed in said semiconductor substrate;

said bulk region including:

a first memory cell array having a plurality of memory cells arranged in the form of a matrix and including a plurality of memory cells connected to bit lines and word lines;

first sense amplifiers connected to said bit lines of said first memory cell array, said first sense amplifiers being adapted to sense and amplify the potentials of said bit lines;

first column selection gates for connecting said first sense amplifiers to first data lines;

a second memory cell array having a plurality of memory cells arranged in the form of a matrix and including a plurality of memory cells connected to bit lines and word lines;

second sense amplifiers connected to said bit lines of said second memory cell array, said second

sense amplifiers being adapted to sense and amplify the potentials of said bit lines; and

second column selection gates for connecting said second sense amplifiers to first data lines;

said semiconductor region including:

first word line selection circuits for selecting appropriate ones of said word lines of said first memory cell array;

second word line selection circuits for selecting appropriate ones of said word lines of said second memory cell array;

first column selection circuits for selecting appropriate ones of said first column selection gates; and

second column selection circuits for selecting appropriate ones of said second column selection gates.

5. The device according to claim 4, further comprising:

third sense amplifiers arranged in said bulk region and connected to said first data lines, said third sense amplifiers being adapted to sense and amplify the potentials of said first data line.

6. The device according to claim 5, further comprising:

first data line drive circuits arranged in said semiconductor region, said first data line drive circuits being adapted to drive said first data lines;

second data line drive circuits arranged in said semiconductor region and connected to said third sense amplifiers, said second data line drive circuits being adapted to drive second data lines according to the output signals of said third sense amplifiers; and

data line control circuits arranged in said semiconductor region and adapted to control said first and second data line drive circuits.

7. The device according to claim 4, further comprising:

switch circuits arranged in said semiconductor region, said switch circuits being adapted to switch from defective first data lines to spare first data lines.

8. The device according to claim 6, further comprising:

a plurality of memory regions containing respectively bulk regions and semiconductor regions, said second data line driving circuits contained in said memory regions being commonly connected to said second data lines.

9. The device according to claim 8, wherein

said bulk regions in said memory regions have substantially the same size.

10. The device according to claim 9, wherein

said memory regions have substantially the same size.

11. The device according to claim 10, further comprising:

a first memory region part containing m memory regions; and

a second memory region part containing n memory regions (m and n being integers and m is greater than or equal to n);

said first and second memory region parts being arranged in a semiconductor chip.

12. The device according to claim 11, wherein said m memory regions are arranged in the direction of said second data lines and said n memory regions are also arranged in the direction of said second data lines.

13. The device according to claim 11, wherein said m memory regions in said first memory region part are arranged in a direction perpendicular to the direction of arrangement of said n memory regions in said second memory region part.

14. The device according to claim 11, wherein at least one of said memory regions is arranged in a semiconductor chip with a logic circuit.

15. A semiconductor device comprising a substantially rectangular bulk region formed in a semiconductor substrate; and

a semiconductor region arranged along three sides of said bulk region, said semiconductor region being

formed on one of a buried insulating film in said semiconductor substrate and a cavity formed in said semiconductor substrate;

said bulk region including:

first and second memory cell arrays having a plurality of memory cells arranged in the form of a matrix and connected to bit lines and word lines;

first sense amplifiers connected to said bit lines of said first memory cell array, said first sense amplifiers being adapted to amplify the potentials of said bit lines;

second sense amplifiers connected to said bit lines of said second memory cell arrays, said second sense amplifiers being adapted to amplify the potentials of said bit lines;

first column selection gates for connecting said first sense amps to the first data lines; and

second column selection gates for connecting said second sense amplifiers to the second data lines;

said semiconductor region including;

a first semiconductor region part arranged along one of a pair of parallel sides of said bulk region;

a second semiconductor region part arranged along the other of the pair of parallel sides;

a third semiconductor region part arranged between said first and second semiconductor region parts;

first word line selection circuits arranged in

said first semiconductor region part; said first word line selection circuits being adapted to select appropriate ones of said word lines of said first memory cell array;

second word line selection circuits arranged in said second semiconductor region part, said second word line selection circuits being adapted to select appropriate ones of said word lines of said second memory cell array; and

column selection circuits arranged in said first semiconductor region part, said column selection circuits being adapted to select appropriate ones of said first and second column selection gates.

16. A semiconductor device comprising:

a bulk region formed in a semiconductor substrate;

a semiconductor region formed on one of a buried insulating film in said semiconductor substrate and a cavity region formed in said semiconductor substrate;

first circuits formed in said bulk region;

transistors formed in said semiconductor regions, said transistors being adapted to generate a first supply voltage out of the supply voltage, said first supply voltage being lower than said supply voltage and applied to said first circuits; and

a control circuit formed in said bulk region and adapted to generate the respective gate voltages of said transistors.

17. The device according to claim 16, wherein said first circuits are sense amplifiers.

18. A semiconductor device comprising:

a bulk region formed in a semiconductor substrate; and

a semiconductor region formed on one of a buried insulating film in said semiconductor substrate and a cavity region formed in said semiconductor substrate;

said bulk region containing memories and read-out circuits of said memories;

said semiconductor region containing write-in circuits of said memories.

19. The device according to claim 18, wherein said bulk region is substantially rectangular shape and said semiconductor region is located along two sides of said bulk region.

20. The device according to claim 18, wherein said semiconductor region contains a switch circuit for switching from defective first data lines to spare first data lines.

21. A semiconductor device formed in a region other than the bulk region within a semiconductor substrate, said device comprising:

a delay circuit adapted to be supplied with a clock signal and delay the clock signal;

a logic circuit adapted to be supplied with the output signal of said delay circuit and said clock

signal;

said delay circuit including:

an inverter circuit for receiving said clock signal;

a capacitor to be charged and discharged in response to the operation of said inverter circuit; and

a transistor connected to said capacitor and the output terminal of said inverter circuit, said transistor being turned off in response to a fall of the output voltage of said inverter circuit under the threshold voltage of said inverter circuit.

22. The device according to claim 21, wherein said capacitor is inserted between the output terminal of said inverter circuit and the ground and said transistor is a P-channel MOS transistor.

23. The device according to claim 21, wherein said capacitor is inserted between the output terminal of said inverter circuit and the power source and said transistor is a N-channel MOS transistor.

24. The device according to claim 22, wherein said capacitor is a MOS capacitor.

25. A semiconductor device formed in a region other than the bulk region within a semiconductor substrate, said device comprising:

a delay circuit for delaying a signal;

first and second latch circuits for alternately holding the output signal of said delay circuit in

response to a clock signal, said second latch circuit being adapted to supply the signal held by itself to said delay circuit;

said delay circuit including:

an inverter circuit for receiving the output signal of said second latch circuit; and

a capacitor connected to the output terminal of said inverter circuit.

26. The device according to claim 25, wherein said first latch circuit is a first flip-flop circuit formed by using two NAND circuits.

27. The device according to claim 25, wherein said second latch circuit is a second flip-flop circuit formed by using two OR circuits.

28. The device according to claim 25, wherein said second latch circuit is a third flip-flop circuit formed by using two NAND circuits, said third flip-flop circuit having first and second input terminals, said first input terminal being adapted to be supplied with an inverted clock signal, said second input terminal being adapted to be supplied with an inverted output signal of said first flip-flop circuit.

29. The device according to claim 28, wherein said third latch circuit includes a 3-input NAND circuit and the output signal of said inverter circuit is directly supplied to the first input terminal of said 3-input NAND circuit.

30. The device according to claim 25, wherein said first and second latch circuits being master/slave type delay flip-flop circuits.

31. The device according to claim 25, further comprising:

a transistor connected between the output terminal of said inverter circuit and the said capacitor, said transistor being turned off when the output signal of said inverter circuit is lower than the threshold voltage of said inverter circuit.

32. The device according to claim 25, wherein said capacitor is a MOS capacitor.